AX5320P

6 Channel
Analog Output Board

User's Manual

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June 2002, Version A2
Printed in Taiwan

ESD Precautions

Integrated circuits on computer boards are sensitive to static electricity. To avoid damaging chips from electrostatic discharge, observe the following precautions:

- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before handling a board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. This helps to discharge any static electricity on your body.
- Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components.

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Unpacking

The AX5320P is packed in an anti-static bag. The PCI Bus board has components that are easily damaged by static electricity. Do not remove the anti-static wrapping until proper precautions have been taken. Safety instructions in front of this User's Manual describe anti-static precautions and procedures.

After unpacking the PCI Bus board, place it on a raised surface and carefully inspect the board for any damage that might have occurred during shipment. Ground the board and exercise extreme care to prevent damage to the board from static electricity.

Integrated circuits will sometimes come out of their sockets during shipment. Examine all integrated circuits, to ensure that they are firmly seated. The AX5320P PCI Bus interface analog output board package includes the following:

- AX5320P Board
- AX5003 Extension Board
- Flat cable 40p 45cm x 1
- AS59099 DAC Driver CD
- Ax5320P user's manual
- Warranty card

Make sure that all of the items listed above are present.

What To Do If There Is A Problem

If there are damaged or missing parts, contact your supplier and/or dealer immediately. Do not attempt to apply power to the board if there is damage to any of its components.

Table of Contents

Chapter 1 Intorduction ---------- 1
1.1 General Description 1
1.2 Specifications 2
1.2.1 D/A 2
1.2.2 Digital Input and Output 3
1.2.3 Power Consumption 3
1.2.4 Physical/Environmental 3
Chapter 2 Board Configuration and Installation ---------- 5
2.1 Locator Diagram 5
2.2 Jumper Settings 6
2.2.1 JP1 ~ JP12 6
2.2.2 J1 ~ J6 6
2.3 Code Format 7
2.3.1 Unipolar Output 7
2.3.2 Bipolar Output 7
2.3.3 Current Sink (4 to 20 mA) 8
2.3.4 Current Sink (0 to 20 mA) 8
2.4 Connector Pin Assignments 9
2.4.1 CON1 Pin Assignments 9
2.4.2 CON2 Pin Assignments 10
2.4.3 P1 Pin Assignments 11
2.5 Hardware Installation 12
2.5.1 Board Installation 12
2.5.2 AX5320P Extension Board Cable Connection 13
Chapter 3 Register Format and Description -15
3.1 I/O Address Mapping 15
3.2 Register Description 16
3.2.1 Group_0 Registers 17
3.2.2 Group_1 registers 18

Chapter 4 Calibration ----------19
4.1 D/A Calibration 19
4.1.1 Voltage Output (Unipolar 0 ~ 5V).....19
4.1.2 Voltage Output (Unipolar 0 ~ 10V).....20
4.1.3 Voltage Output (Bipolar - 5 ~ + 5V).....20
4.1.4 Voltage Output (Bipolar - 10 ~ + 10V).....21
4.1.5 Current Sink(0 ~ 20mA).....21
4.1.6 Current Sink(4 ~ 20mA).....22
Appendix A Block Diagram ----------23

Chapter 1
Introduction

1.1 General Description

The AX5320P is a PCI card providing 6 channels analog output and 8 digital inputs, and/or 8 digital outputs. The board interface allows its plugging into any PCI slot of an IBM™ PC/AT or compatible computer with PCI bus.

The AX5320P features 6 channels of voltage output or current sink, each channel is individually user selectable to any of the following ranges: 0 to 5V, 0 to 10V, -5V to +5V, -10V to +10V, 0 to 20 mA or 4 to 20 mA current loop. There is one 12-bit D/A converter per channel for maximum 33KHz throughput. Typical applications for AX5320P include ON/OFF control, direct control valve positioning, waveform generation and utilizing a variable voltage output. The board can also be used for analog control in process or laboratory application where material transfer rates, fluid flow, power consumption, motor speed, temperature levels, etc., are to be controlled. Optional AX851 universal terminal panel is available to help facilitate external connections.

1.2 Specifications

1.2.1 D/A

- **Analog Outputs**
  - Number of channels: 6
  - Output Ranges: 0 to 5V, 0 to 10V, ±5V, ±10V
0-20mA, 4-20mA current sink
  - Input data coding: Straight binary (unipolar)
Offset binary (bipolar)
  - Current Output, Voltage range: +/-5mA max.
  - Source Impedance: 0.1 Ω max.
0.02 Ω typ.
  - Capacitive Driver Capability: short circuit to common
  - Protection: for voltage ranges, current outputs are short circuit, and reverse polarity protected.
- **Accuracy**
  - Resolution: 12 bits
  - Nonlinearity: +/- 1 LSB
  - Differential Nonlinearity: +/- 1/2 LSB
  - Inherent quantizing Error: +/- 1/2 LSB
  - Gain Error: Adjustable to zero
  - Zero Error: Adjustable to zero
  - System Accuracy: +/- 0.025%FSR (Voltage out)
+/- 0x05%FSR(Current out)
- **Dynamic Performance**
  - Settling Time to 1/2 LSB
    - (10V step): 33µs
    - (5V step): 16µs
  - Slew Rate: 0.3V/µs TYP(voltage)
1.2mA/µs(current)
  - DAC Throughput
    - Single Channel33kHz

- **Thermal Characteristics**
  - Zero Drift: +/- 10µV/°C
  - Gain Drift: +/-20ppm of FSR/°C
  - Differential Linearity Drift: +/-3ppm of FSR/°C
  - Monotonicity: Monotonic,0 to +60°C

1.2.2 Digital Input and Output

- Input Lines: 8
- Output Lines: 8
- Input/Output level: TTL/DTL compatible
- Electrical Characteristics
  - Logic High Input Voltage: 2V (MIN.)
  - Logic Low Input Voltage: 0.8V (MAX.)
  - Logic High Input Current: 20µA (MAX.) at VIH=2.7V
  - Logic Low Input Current: -0.2mA (MAX.) at VIL=0.4V
  - Logic High Output Voltage: 2.4V (MIN.) at IOH=-3mA
  - Logic Low Output Voltage: 0.4V (MAX.) at IOL=12mA
  - Logic High Output Current: -0.4 mA source (MAX.)
  - Logic Low Output Current: 8 mA Sink (MAX.)

1.2.3 Power Consumption

- **+5V:** 200mA
- **+12V:** 300mA

1.2.4 Physical/Environmental

- **I/O Connector:** 37-pin D-type male connector
  40-pin male mating connector
- **Dimensions:** 175mm*106mm
- **Weight:** 270g
- **Operating temp Range:** 0°C to 70°C
- **Relative Humidity:** 0 to 90%; non-condensing

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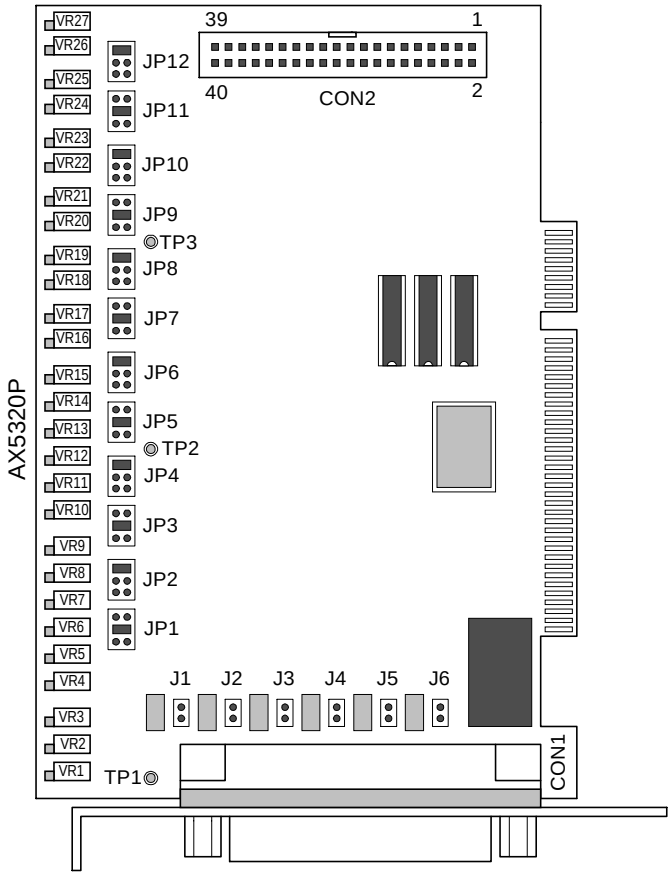
Chapter 2
Board Configuration and Installation

WARNING: *When power is ON, hazardous voltages may be present in the AX5320P, do not touch the board and its wiring to prevent shock hazard*

2.1 Locator Diagram

The following figure shows locations of jumpers and connectors.



2.2 Jumper Settings

2.2.1 JP1 ~ JP12

JP1(DA1), JP3(DA2), JP5(DA3), JP7(DA4), JP9(DA5), JP11(DA6)

Set DA channel to be current sink

Set DA channel to be unipolar (voltage output)

Set DA channel to be bipolar (voltage output)

JP2(DA1), JP4(DA2), JP6(DA3), JP8(DA4), JP10(DA5), JP12(DA6)

Select DA reference voltage = external voltage

Select DA reference voltage = -10V

Select DA reference voltage = -5V or Current Sink

2.2.2 J1 ~ J6

J1(DA1), J2(DA2), J3(DA3), J4(DA4), J5(DA5), J6(DA6)

	Set DA as voltage output or current loop 0 ~ 20 mA
	Set DA as current sink 4 ~ 20 mA

2.3 Code Format

There are three kinks of reference voltage input (-5V, -10V and external) can be selected by the jumper JP2, JP4, JP6, JP8, JP10, JP12. When the voltage reference (Vref) is selected, this channel's D/A voltage output range is from 0V to |Vref| for unipolar (UNI), -|Vref| to |Vref| for biplar (BIP). The reference signal can be DC or AC voltage. In this way, the D/A becomes a programmable atenuator. The equation for calculating output is:

DAV = |Vref| *[code/4096]

Where code is the data written to the D/A register, the range is between 0 to 4095.

2.3.1 Unipolar Output

DAV = |Vref| *[code/4096]

Binary Number in DAC		Analog Output, DAV
MSB	LSB	
1 1 1 1 1 1 1 1	1 1 1 1	|Vref| *[4095/4096]
1 0 0 0 0 0 0 0	0 0 0 0	|Vref|*[2048/4096]=1/2|Vref|
0 0 0 0 0 0 0 0	0 0 0 1	|Vref|*[1/4096]
0 0 0 0 0 0 0 0	0 0 0 0	0 Volts

2.3.2 Bipolar Output

DAV = |Vref| *[(code – 2048)/4096]

Binary Number in DAC		Analog Output, DAV
MSB	LSB	
1 1 1 1 1 1 1 1	1 1 1 1	|Vref| *[2047/2048]
1 0 0 0 0 0 0 0	0 0 0 1	|Vref|*[1/2048]
1 0 0 0 0 0 0 0	0 0 0 0	0 Volts
0 1 1 1 1 1 1 1	1 1 1 1	-|Vref|*[1/2048]
0 0 0 0 0 0 0 0	0 0 0 0	-|Vref|

2.3.3 Current Sink (4 to 20 mA)

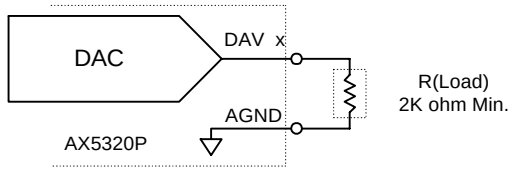
Current Sink(mA) = 4mA + (code/4096) * 16mA

Binary Number in DAC		Current Sink (mA)
MSB	LSB	
0 0 0 0 0 0 0 0	0 0 0 0	4
0 1 0 0 0 0 0 0	0 0 0 0	8
1 0 0 0 0 0 0 0	0 0 0 0	12
1 1 1 1 1 1 1 1	1 1 1 1	19.9961

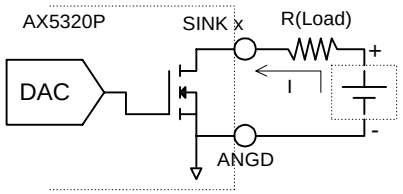
2.3.4 Current Sink (0 to 20 mA)

Current Sink(mA) = (code/4096) * 20mA

Binary Number in DAC		Current Sink (mA)
MSB	LSB	
0 0 0 0 0 0 0 0	0 0 0 0	0
0 1 0 0 0 0 0 0	0 0 0 0	5
1 0 0 0 0 0 0 0	0 0 0 0	10
1 1 1 1 1 1 1 1	1 1 1 1	19.99512



Voltage Output connection



Power supply (6 - 36V) 20mA (Max.)

Current Sink connection

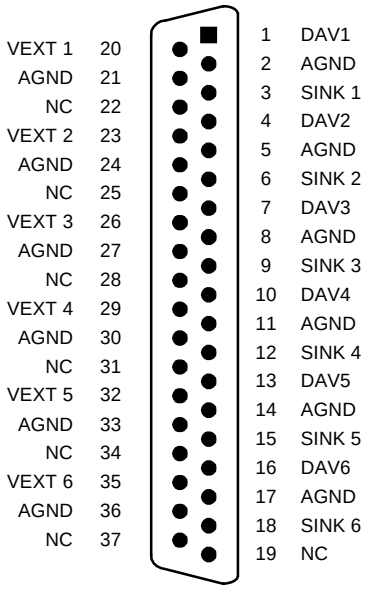
NOTE: *The users must also consider the power consumption (P) on R(Load), where P = I*V*

2.4 Connector Pin Assignments

The AX5320P 6 Channel Analog Output Board has two I/O connectors labeled CON1 and CON2 accessible from the expansion slot rear panel of the PC. The pin assignments for CON1 and CON2 are listed on the following subsections.

2.4.1 CON1 Pin Assignments

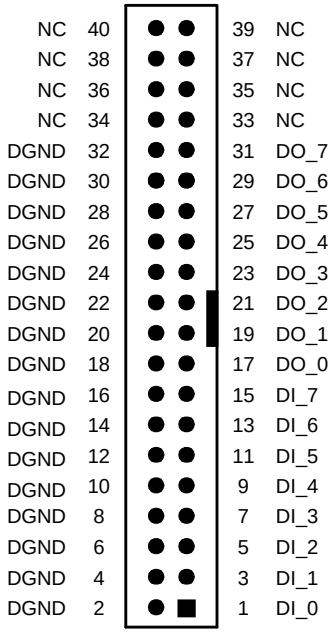
CON1



Pin Name	Description (CON1)
N/C	No connect
AGND	Analog ground
DAV1~DAV6	D/A voltage output channel_1 to channel_6
SINK1~SINK6	D/A current sink channel_1 to channel_6

2.4.2 CON2 Pin Assignments

CON2



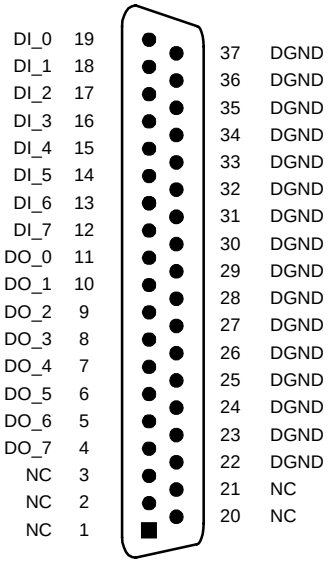
Pin Name	Description (CON2)
N/C	No connect
DI_0~DI_7	Digital input channel_0 ~ channel_7
DO_0~DO_7	Digital output channel_0 ~ channel_7

2.4.3 P1 Pin Assignments

A cable connector to convert the CON2 (40-pin connector) to 37-pin male D-type connector is given along with the AX5320P board. Description for the cable connector is provided below.

AX5320P extension board AX5003 pin assignment

P1



Pin Name	Description (CON2)
DI_0~DI_7	Digital input channel_0 ~ channel_7
DO_0~DO_7	Digital output channel_0 ~ channel_7

2.5 Hardware Installation

The AX5320P board is shipped with protective electrostatic cover. When unpacking, touch the board's electrostatically shielded packing with the metal frame of your computer to discharge the accumulated static electricity prior to touching the board.

The following section summarizes the procedures when installing the AX5320P:

WARNING: *Turn OFF the PC and all accessories connected to the PC whenever installing or removing any peripheral board including the AX5425(0) series board.*

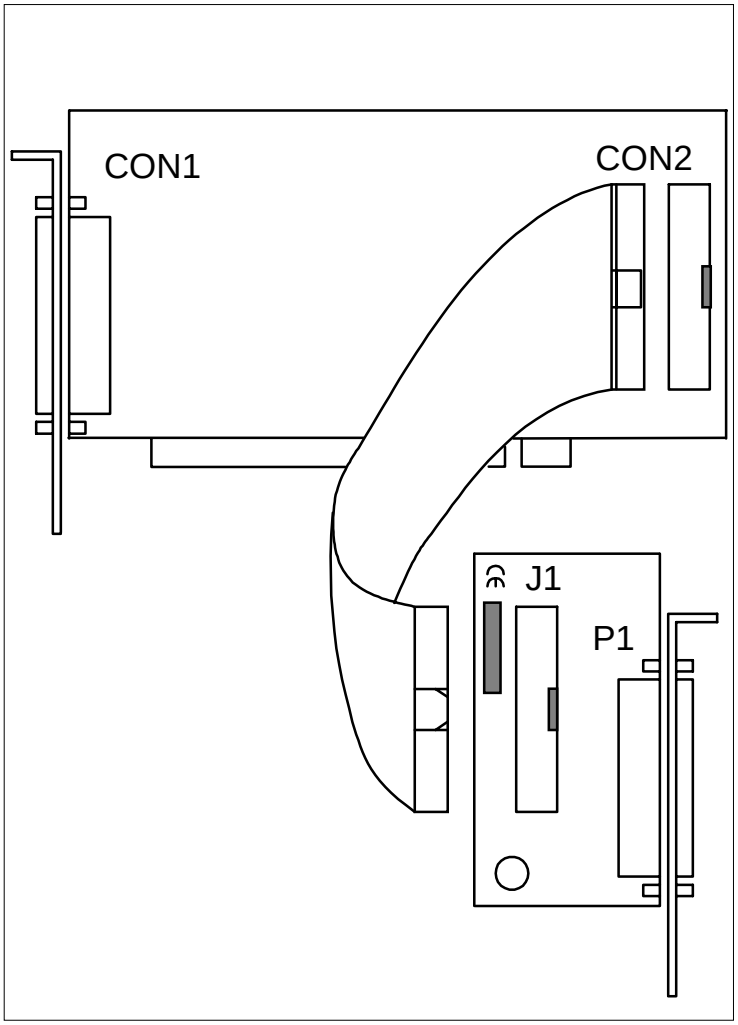
2.5.1 Board Installation

The following lists the instructions to follow when installing the AX5320P card.

1. Turn OFF the PC and all accessories power.
2. Unplug all power cords and entire cables from the rear of the PC.
3. Remove the PC's cover (see your PC Operation Guide if you are not skillful about it).
4. Find an unused expansion slot. Remove the blank expansion slot cover and save the screw for affixing retaining bracket.
5. Grab the upper edge of the AX5320P board. Align the AX5320P board's retaining bracket with the expansion slot rear panel, and straighten the board's gold finger with the expansion slot. Gently push the board into slot.
6. Restore the screw to the expansion slot-retaining bracket.
7. Replace the PC's cover and connect the cables you detached in step2.
8. Turn ON the power of the PC and other peripheral device.

2.5.2 AX5320P Extension Board Cable Connection

Refer to the following illustration for the proper cable connection from the AX5320P card to the AX5003 extension board.



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Chapter 3
Register Format and Description

3.1 I/O Address Mapping

The AX5320P use some non-consecutive addresses in I/O space. All registers are 8 bits wide. The base address (or starting address) is determined during the installation by CPU auto setting. This chapter describes each register's format and functions. Each register can be accessed easily by using direct I/O instructions of whatever application languages available (Assembly, Basic, Pascal, C, etc.). Don't operate any other I/O(NOT LISTED) , or else it happens errors.

Location	Function	Type
Base Address + 0	Enable external reset	W
Base Address + 2	Group select control	W
Base Address + 3	Group select control	W
Base Address + 7	Group select control register status	R

GROUP 0

Location	Function	Type
Base Address + 0xc0	D/A 1 Low byte	W
Base Address + 0xc4	D/A 1 High byte	W
Base Address + 0xc8	D/A 2 Low byte	W
Base Address + 0xcc	D/A 2 High byte	W
Base Address + 0xd0	D/A 3 Low byte	W
Base Address + 0xd4	D/A 3 High byte	W
Base Address + 0xd8	D/A 4 Low byte	W
Base Address + 0xdc	D/A 4 High byte	W
Base Address + 0xe0	D/A 5 Low byte	W
Base Address + 0xe4	D/A 5 High byte	W
Base Address + 0xe8	D/A 6 Low byte	W
Base Address + 0xec	D/A 6 High byte	W

GROUP 1

Location	Function	Type
Base Address + 0xc0	8 channels digital input	W
Base Address + 0xc0	8 channels digital output	R

3.2 Register Description

Base address + 0 (write)

X	X	X	X	X	X	X	RST

RST = 0 disable RESET function on AX5320P
RST = 1 enable RESET function on AX5320P, when system (PC) reset, the AX5320P will be reset.

Base address + 2 (write)

X	X	X	IRQ	X	X	SG1	SG0

When the start or initiation of the program, users must output a value 0x03(or 0x0f) to Base Address + 0x02 to set the IRQ signal is input to and the SG0, SG1 are output from the PCI bridge.

Base address + 3 (write)

X	X	X	X	X	X	SG1	SG0

SG1, SG0 are action low

SG1	SG0	Description
1	0	Select/Enable Group 0
0	1	Select/Enable Group 1

Base address + 7 (read)

X	X	X	IRQ	X	X	SG1	SG0

Group selects control register status.

3.2.1 Group_0 Registers

NOTE: *When users program the registers in Group_0, they must check if the I/O port Base address + 2 has an output value 0x03(or 0x0f), and the I/O port Base address + 3 has an output value 0x02 to enable the functions in Group_0.*

Base address + 0xc0 D/A 1 Low byte

B4	B3	B2	B1	X	X	X	X

Base address + 0xc4 D/A 1 high byte

B12	B11	B10	B9	B8	B7	B6	B5

Base address + 0xc8 D/A 2 Low byte

B4	B3	B2	B1	X	X	X	X

Base address + 0xcc D/A 2 high byte

B12	B11	B10	B9	B8	B7	B6	B5

Base address + 0xd0 D/A 3 Low byte

B4	B3	B2	B1	X	X	X	X

Base address + 0xd4 D/A 3 High byte

B12	B11	B10	B9	B8	B7	B6	B5

Base address + 0xd8 D/A 4 Low byte

B4	B3	B2	B1	X	X	X	X

Base address + 0xdc D/A 4 High byte

B12	B11	B10	B9	B8	B7	B6	B5

Base address + 0xe0 D/A 5 Low byte

B4	B3	B2	B1	X	X	X	X

Base address + 0xe4 D/A 5 High byte

B12	B11	B10	B9	B8	B7	B6	B5

Base address + 0xe8 D/A 6 Low byte

B4	B3	B2	B1	X	X	X	X

Base address + 0xec D/A 6 High byte

B12	B11	B10	B9	B8	B7	B6	B5

3.2.2 Group_1 registers

NOTE: *When users program the registers in Group_1, they must check if the I/O port Base address + 2 has an output value 0x03(or 0x0f), and the I/O port Base address + 3 has an output value 0x01 to enable the functions in Group_1.*

Base address + 0xc0 8 channels D/I

DI_7	DI_6	DI_5	DI_4	DI_3	DI_2	DI_1	DI_0

Base address + 0xc0 8 channels D/O

DO_7	DO_6	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0

Chapter 4
Calibration

4.1 D/A Calibration

D/A adjustment is executed for AX5320P D/A calibration.The D/A output voltage can be measured by a DVM or directly to other AXIOMTEK's A/D cards.

Step 1: Connect TP1(+) and AGND(-) to multimeter(recmmend HP34401A). Trim VR1 to measure the voltage equal +2.5000V.

Step 2: Connect TP2(+) and AGND(-), trim VR3 to measure the voltage equal –10.0000V.

Step 3: Connect TP3(+) and AGND(-), trim VR2 to measure the voltage equal –5.0000V.

Step 4: Run the calibration program cal5320p.exe and conform it.

4.1.1 Voltage Output (Unipolar 0 ~ 5V)

	DAV1	DAV2	DAV3	DAV4	DAV5	DAV6	
Set	JP1	JP3	JP5	JP7	JP9	JP11	Unipolar
Set	JP2	JP4	JP6	JP8	JP10	JP12	Vref=-5V
Base + Output	0xc0 0xf0	0xc8 0xf0	0xd0 0xf0	0xd8 0xf0	0xe0 0xf0	0xe8 0xf0	D/A Low Byte
Base + Output	0xc4 0xff	0xcc 0xff	0xd4 0xff	0xdc 0xff	0xe4 0xff	0xec 0xff	D/A High Byte
Trim	VR16	VR18	VR20	VR22	VR24	VR26	Measure 4.99878V

4.1.2 Voltage Output (Unipolar 0 ~ 10V)

	DAV1	DAV2	DAV3	DAV4	DAV5	DAV6	
Set	JP1	JP3	JP5	JP7	JP9	JP11	Unipolar
Set	JP2	JP4	JP6	JP8	JP10	JP12	Vref=-10V
Base + Output	0xc0 0xf0	0xc8 0xf0	0xd0 0xf0	0xd8 0xf0	0xe0 0xf0	0xe8 0xf0	D/A Low Byte
Base + Output	0xc4 0xff	0xcc 0xff	0xd4 0xff	0xdc 0xff	0xe4 0xff	0xec 0xff	D/A High Byte
Trim	VR16	VR18	VR20	VR22	VR24	VR26	Measure 9.99756V

4.1.3 Voltage Output (Bipolar - 5 ~ + 5V)

	DAV1	DAV2	DAV3	DAV4	DAV5	DAV6	
Set	JP1	JP3	JP5	JP7	JP9	JP11	Bipolar
Set	JP2	JP4	JP6	JP8	JP10	JP12	Vref=-5V
Base + Output	0xc0 0x00	0xc8 0x00	0xd0 0x00	0xd8 0x00	0xe0 0x00	0xe8 0x00	D/A Low Byte
Base + Output	0xc4 0x00	0xcc 0x00	0xd4 0x00	0xdc 0x00	0xe4 0x00	0xec 0x00	D/A High Byte
trim	VR17	VR19	VR21	VR23	VR25	VR27	Measure –5V
Base + output	0xc0 0xf0	0xc8 0xf0	0xd0 0xf0	0xd8 0xf0	0xe0 0xf0	0xe8 0xf0	D/A Low Byte
Base + Output	0xc4 0xff	0xcc 0xff	0xd4 0xff	0xdc 0xff	0xe4 0xff	0xec 0xff	D/A High Byte
Trim	VR16	VR18	VR20	VR22	VR24	VR26	Measure +4.99756V

4.1.4 Voltage Output (Bipolar - 10 ~ + 10V)

	DAV1	DAV2	DAV3	DAV4	DAV5	DAV6	
Set	JP1	JP3	JP5	JP7	JP9	JP11	Bipolar
Set	JP2	JP4	JP6	JP8	JP10	JP12	Vref=-10V
Base + Output	0xc0 0x00	0xc8 0x00	0xd0 0x00	0xd8 0x00	0xe0 0x00	0xe8 0x00	D/A Low Byte
Base + Output	0xc4 0x00	0xcc 0x00	0xd4 0x00	0xdc 0x00	0xe4 0x00	0xec 0x00	D/A High Byte
Trim	VR17	VR19	VR21	VR23	VR25	VR27	Measure –10V
Base + Output	0xc0 0xf0	0xc8 0xf0	0xd0 0xf0	0xd8 0xf0	0xe0 0xf0	0xe8 0xf0	D/A Low Byte
Base + Output	0xc4 0xff	0xcc 0xff	0xd4 0xff	0xdc 0xff	0xe4 0xff	0xec 0xff	D/A High Byte
Trim	VR16	VR18	VR20	VR22	VR24	VR26	Measure +9.99512V

4.1.5 Current Sink(0 ~ 20mA)

	SINK1	SINK2	SINK3	SINK4	SINK5	SINK6	
Set	JP1	JP3	JP5	JP7	JP9	JP11	Current Sink
Set	JP2	JP4	JP6	JP8	JP10	JP12	Vref=-5V
Set	J1	J2	J3	J4	J5	J6	Open
Base + Output	0xc0 0xf0	0xc8 0xf0	0xd0 0xf0	0xd8 0xf0	0xe0 0xf0	0xe8 0xf0	D/A Low Byte
Base + Output	0xc4 0xff	0xcc 0xff	0xd4 0xff	0xdc 0xff	0xe4 0xff	0xec 0xff	D/A High Byte
Trim	VR4	VR5	VR6	VR7	VR8	VR9	Measure 20.0mA

4.1.6 Current Sink(4 ~ 20mA)

	SINK1	SINK2	SINK3	SINK4	SINK5	SINK6	
Set	JP1	JP3	JP5	JP7	JP9	JP11	Current Sink
Set	JP2	JP4	JP6	JP8	JP10	JP12	Vref=-5V
Set	J1	J2	J3	J4	J5	J6	Short
Base + Output	0xc0 0xf0	0xc8 0xf0	0xd0 0xf0	0xd8 0xf0	0xe0 0xf0	0xe8 0xf0	D/A Low Byte
Base + Output	0xc4 0xff	0xcc 0xff	0xd4 0xff	0xdc 0xff	0xe4 0xff	0xec 0xff	D/A High Byte
Trim	VR4	VR5	VR6	VR7	VR8	VR9	Measure 20.0mA
Base + Output	0xc0 0x00	0xc8 0x00	0xd0 0x00	0xd8 0x00	0xe0 0x00	0xe8 0x00	D/A Low Byte
Base + Output	0xc4 0x00	0xcc 0x00	0xd4 0x00	0xdc 0x00	0xe4 0x00	0xec 0x00	D/A High Byte
Trim	VR10	VR11	VR12	VR13	VR14	VR15	Measure 4.0mA

Appendix A
Block Diagram